Section 5 – Digital Circuitry

5.1 Classes
- Bipolar Junction Transistors (BJTs)
  - TTL, LTTL, STTL, LSTTL
  - ECL, I(ntegrated)I(njection)L, D(Diode)TL
- Metal Oxide Semiconductor (MOS)
  - PMOS, NMOS, CMOS

5.2 Operational Parameters

5.2.1 Voltage & Current

\[ V_{xy} \Rightarrow \text{Voltage x defined as either Input or Output} \]
\[ => \text{Voltage y defines either logic high or low} \]
\[ I_{xy} \Rightarrow \text{Current x defined as either Input or Output} \]
\[ => \text{Current y defines either logic high or low} \]

\[ V_{IH} \Rightarrow \text{Min voltage at input which can be ‘read’ as a 1(high)} \]
\[ V_{IL} \Rightarrow \text{Max voltage at input which can be ‘read’ as a 0(low)} \]
\[ V_{OH} \Rightarrow \text{Min voltage at output which allows a 1(high)} \]
\[ V_{OL} \Rightarrow \text{Max voltage at output which can be ‘read’ as a 0(low)} \]

\[ I_{IH} \Rightarrow \text{Input current when input = 1} \]
\[ I_{IL} \Rightarrow \text{Input current when input = 0} \]
\[ I_{OH} \Rightarrow \text{Output current when output = 1} \]
\[ I_{OL} \Rightarrow \text{Output current when output = 0} \]
5.2.2 Fan-out

- Max amount of inputs driven by output.

Example
Determine the Fan-out of an NAND only circuit given the following values:

\[ I_{OH} = 400 \, \mu A, \quad I_{IH} = 60 \, \mu A, \quad I_{OL} = 16 \, mA, \quad I_{IL} = 1.6 \, mA \]

During high condition =>
Each NAND gate provides 400 \, \mu A current at output
Each NAND gate sources 60 \, \mu A current at input.
Fan-out\textsubscript{HIGH} = \frac{I\text{OH}}{I\text{IH}} = \frac{400}{60} = 6
\text{(Rounded down since cannot drive part of a gate!)}

During low condition =>
Each NAND gate provides 16 mA current at output
Each NAND gate sources 1.6 mA current at input.

Fan-out\textsubscript{LOW} = \frac{I\text{OL}}{I\text{IL}} = \frac{16}{1.6} = 10

Fan-out of NAND gate is the lower value…
\Rightarrow \text{Fan-out} = 6

5.2.3 Propagation Delays

\begin{itemize}
  \item Delay when switching from one logic level to another

\begin{center}
\begin{tikzpicture}
  \node at (-1,0.5) {Input};
  \node at (0,0.5) {0};
  \node at (2,0.5) {1};
  \node at (0,-0.5) {Output};
  \node at (-1,-0.5) {0};
  \node at (2,-0.5) {1};
  \draw (0,0) -- (2,0);
  \draw (0,-0.5) -- (2,-0.5);
  \draw (0,0) -- (0,-0.5);
  \draw (2,0) -- (2,-0.5);
  \draw[dashed] (0.5,-0.5) -- (0.5,-0.75);
  \draw[dashed] (1.5,-0.5) -- (1.5,-0.75);
  \draw[dashed] (0.5,0) -- (0.5,0.25);
  \draw[dashed] (1.5,0) -- (1.5,0.25);
  \node at (0.5,-1) {t\text{PHL}};
  \node at (1.5,-1) {t\text{PLH}};
\end{tikzpicture}
\end{center}

\begin{itemize}
  \item t\text{PHL} = Falling delay, delay incurred when output changes from High to Low.
  \item t\text{PLH} = Rising delay, delay incurred when output changes from Low to High.
\end{itemize}
5.2.4 Power Requirements

- **Usually the supply current $I_{CC}$ is given**
  \[ \text{Power} = V_{cc} \times I_{cc} \]

- OR
  - $I_{CCH}$ and $I_{CCL}$ are given.
    - $I_{CCH} : I_{CC}$ when all outputs HIGH
    - $I_{CCL} : I_{CC}$ when all outputs LOW

- Power determined by speed
  - Charging and Discharging of Capacitances, etc.

5.2.5 Noise Immunity

- **Circuit must be able to tolerate some noise at input without error**

- **Calculate Noise Immunity of Circuit**
  - Determine ‘how much’ Input Noise voltage can be tolerated without change in output state
  - Must be determined for both positive and negative noise
• When output is HIGH, Noise voltages more Negative than $V_{NL}$ will push output into undetermined value
  ○ $V_{NL} = V_{IL} - V_{OL}$

• When output is LOW, Noise voltages more Positive than $V_{NH}$ will push output into undetermined value

5.3 Transistor Transistor Logic (TTL)

• Uses Bipolar Junction Transistors (BJT) & Resistors to form logic function
• Transistors used to perform logic and signal modification

5.3.1 TTL Configurations

• Standard TTL
  ▪ Logic 0 : 0V-0.8V $V_{IL}$
  ▪ Logic 1 : 2V-5V $V_{IH}$
  ▪ Switching speed : ~10nS
  ▪ Power Consumption : 10mW

• High Speed
  ▪ Improved (HS)-TTL Transistor (6nS : 22mW)
  ▪ Schottky TTL (3nS : ~22mW)

• Low Power
  ▪ Low Power TTL
  ▪ Improved (LP)- Schottky
  ▪ Low Voltage (LV)-TTL ($V_{DD}$=3.3V)

5.3.2 TTL Outputs

▪ Totem-Pole Output
▪ Open Collector Output
▪ Tri-State Output
5.3.3 Standard TTL

5.3.3.1 74XX TTL Inverter

When A is high (>2V)
- Q1 has reverse biased base emitter
- Current Flows through base of Q1 into base of Q2 (Q2B)
- Q2 is ON, pulling F to GND.

When A is low (<0.8V)
- Q1 has forward biased base emitter
- Current charge in Q2B is discharged through A, turning Q2 OFF. \( I_L = -1.6\text{mA} \)
- F pulled high (5 minus voltage drop across resistor)

Properties
- Open Collector Output: Output F ‘floats’ high when input is 0.
- Can only Sink current at output.
- Open Collector output requires a pull up resistor on output to ensure proper logic levels.

Open Collector Resistor
- Try to minimise resistor value to ensure maximum switching speed.
- Minimise voltage swing between 0 and 1
Resistor value:

\[ R \leq \frac{+5 - V_{OUT}}{I_{OUT}} \]

- \( V_{OUT} \) depends on TTL logic levels, must be \( >2.0V \) plus some margin of error.
- \( I_{OUT} \) depends on how many inputs driven by output.
- \( I_{OUT} \) must be greater than \( n*I_{IH} \) where \( I_{IH} \) in the high input current and \( n \) is the number of outputs.

**Example**

Design open collector inverter which must provide TTL logic levels + 100 % tolerance. The output is to drive 3 TTL inputs which have a high input current requirement of 60uA, \( I_{IH} = 60 \text{ uA} \).

\[ V_{OUT} = 2V + 2V = 4V \]

\[ I_{OUT} > 180\text{uA}, \quad \text{Round to } 200\text{uA}. \]

\[ R \leq \frac{5 - 4}{200\text{uA}} \leq 5\Omega \text{ (Max Resistor Size)} \]

**5.3.3.2 TTL NAND**

![TTL NAND Diagram]
When A and B are high (>2V)
- Q1 is reverse biased base emitter
- Current flows through base of Q1 into base of Q2 (Q2B)
- Q2 is ON, pulling Q3B to GND so Q3 is OFF.
- Q4 in ON, pulling F to GND (0.4V)

When either A or B is low (<0.8V)
- Q1 is forward biased base-emitter.
- Q1 is ON, discharging current in Q2B, switching Q2 OFF.
- Q3 is saturated, Pulling F to 5V (minus Voltage drop across resistor & V_{CE} of Q3 : ~3.1V)
- Q4 is OFF

TTL NAND Truth Table

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>0</td>
</tr>
</tbody>
</table>

Properties
- Circuit Uses **Totem Pole Output**.
- Q3 and Q4 provide totem pole outputs.
  - Q3 pulls up and Q4 pulls down.
- Faster than Pull-up Resistor.
- Can Sink and Source current.

- TTL NOR gate follows similar principles
### 5.3.4 TTL Loading Rules

- Needed to determine the Fan-out of a TTL circuit.
- Defines input/output loading conditions in terms of current
  - Unit loads (U.L)
    - 40uA in HIGH state
    - 1.6mA in LOW state
  - Example: TTL Input Rated at 1 U.L
    - Will draw(sink) 40uA when HIGH
    - Will source 1.6mA back when LOW

#### 5.3.4.1 Current Sinking

- Q1 = OFF, Q2 = ON
- Q2 acting as sink for other TTL inputs
- $R_Q$ non-zero => Voltage drop $V_{OL}$ produced
- TTL limits $V_{OL}$(MAX) to 0.4V
  - $I_{OL}$ is limited by $V_{OL}$
  - Fan-out is limited

$I_{OL}$ is limited because $V_{OL}$ must be $\leq 0.4V$
5.3.4.1 Current Sourcing

- Q1 = ON, Q2 = OFF
- Q1 acting as source for other TTL inputs
- If n*I_{IH} is too high, I_{OH} will be too high.
  - Higher I_{OH} = Larger drop across R (right of R1), Q1 and D
  - Lower V_{OH}
- TTL limits V_{OH}(MIN) to 2.4V
  - I_{OH} is limited by V_{OH}
  - Fan-out is limited
5.3.5 Data Busing

- Data Bus forms common path between inputs & outputs of multiple logic circuits

- Allows data to be transferred between logic circuits

- Methods of Data Busing
  1) Wired-AND (using Open-Collector)
  2) Tri-State Logic (usually using totem-pole)

5.3.5.1 Wired-AND

- Connect Open-Collector outputs to shared bus
  - If A or B = 0, Data bus is 0
  - If A = B = 1, Data bus value is 1
  - Bus line performs AND function

- Resistors not needed at every O/P
  - Minimise for speed but maximise to limit $I_{OL_{MAX}}$
  - If A=0, B=1. R must be large enough to ensure sink current is $< I_{OL_{MAX}}$

- To Transfer data
  - Ensure output B is 1
  - Bus Line will track changes in logic value of A
1. When A = 0, Bus Line = 0  
2. When A = 1, Bus Line = 1

Example
Sequence, \( S = 0,1,1,0 \) sent from A along bus:

Suppose: Output from A = 1 and Output from B = 0

- Current Sourced from A and Sunk in B

Current, \( I \), determined by voltage drop across Q1 (top left), D and Q3 (bottom right) Q1 and Q3 = \( V_{CE(SAT)} = 0.2V \), D = 0.7V

\[
I = \frac{(5 - 0.7 - 0.2 - 0.2)}{130} = 30mA
\]
TTL defines $I_{OL}(\text{max}) = 16\text{mA}$, so wired-ANDed TTL current would be more than allowed.

Problem is worse if more than 2 TTL circuits are connected

### 5.3.5.2 Tri-state

- With open collector, bus switches between 0(LOW) and 1 (FLOAT)
- Open collector performance limited by resistor

How to take advantage of totem pole in data-busing?  
Totem-pole has 2 logic levels: 0(LOW) and 1(HIGH)

Additional state added, High impedance

High Impedance (Hi-Z)  
Connection looks like open-circuit  
High Input impedance blocks input current

**Tri-State TTL NAND gate**
<table>
<thead>
<tr>
<th>En</th>
<th>A</th>
<th>B</th>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>~2.4V</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>~2.4V</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>~2.4V</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>~2.4V</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>5V</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>5V</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>5V</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>0V</td>
</tr>
</tbody>
</table>

Only 1 Enable (= !C in Fig) line can be 1 at any time
5.3.6 Schottky TTL

- Uses low forward voltage drop to limit transistor saturation
  - SBD has forward voltage drop of 0.25V
  - Collector-base forward bias by more than 0.25V
  - Stops transistor from going deep into saturation allowing faster switching off (less to discharge).
  - Switching speed further improved by smaller resistors

Schottky TTL Properties
- Propagation delay for single gate reduced to 3nS
- Power dissipation per gate is 23mW

Low Power Schottky TTL
- Increase resistor value to reduce $P_D$ to 2mW
- Gate propagation delay increased to ~9nS
5.4 Emitter Coupled Logic (ECL)

The term ECL stands for Emitter Coupled logic, which is a bipolar circuit technology. ECL has the fastest switching speed of any logic family, but its power consumption is much higher.

ECL Logic Levels:
Logic 1 = -0.8V
Logic 0 = -1.7V

5.4.1: Emitter Coupled Logic inverter/buffer

\[ V_{IN} = -1.7V \text{ (logic 0)} \]
- Q1 is OFF but Q2 is ON.
  \[ V_{C1} = 0 \Rightarrow Q3 \text{ is OFF} \Rightarrow V_{OUT1} = -0.8V \text{ (logic 1)} \]
  \[ V_{C2} = -0.9 \Rightarrow Q4 \text{ is ON} \Rightarrow V_{OUT2} = -1.7V \text{ (logic 0)} \]

\[ V_{IN} = -0.8 \text{ (logic 1)} \]
- Q1 is ON but Q2 is OFF.
  \[ V_{C1} = -0.9 \Rightarrow Q3 \text{ is ON} \Rightarrow V_{OUT1} = -1.7V \text{ (logic 0)} \]
  \[ V_{C2} = 0 \Rightarrow Q4 \text{ is OFF} \Rightarrow V_{OUT2} = -0.8V \text{ (logic 1)} \]
Q1 and Q2 cannot be on at the same time. Neither operates in saturation.

\[ \Rightarrow \text{Faster Switching} \]

Circuit provides both Inversion \((V_{OUT1})\) and buffering \((V_{OUT2})\)

**Q3 and Q4 are emitter follower functions and produce ECL logic levels**

### 5.3: Emitter Coupled Logic OR/NOR

When either \(A\) or \(B\) = -0.8V (logic 1)

- QA or Q1 is ON but Q2 is OFF.
  
  \[ \Rightarrow V_{C1} = -0.9V \Rightarrow Q3 \text{ is ON} \Rightarrow V_{OUT1} = -1.7V (0) \]
  
  \[ \Rightarrow V_{C2} = 0V \Rightarrow Q4 \text{ is OFF} \Rightarrow V_{OUT2} = -0.8V (1) \]

When \(A=B=-1.7\) (logic 0)

- QA and Q1 are OFF but Q2 is ON.
  
  \[ \Rightarrow V_{C1} = 0 \Rightarrow Q3 \text{ is OFF} \Rightarrow V_{OUT1} = -0.8V \text{ (logic 1)} \]
  
  \[ \Rightarrow V_{C2} = -0.9 \Rightarrow Q4 \text{ is ON} \Rightarrow V_{OUT2} = -1.7V \text{ (logic 0)} \]

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>(V_{OUT1})</th>
<th>(V_{OUT2})</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

\[ V_{OUT1} = \overline{A} + B \]

\[ V_{OUT2} = A + B \]
5.4: ECL Properties
Typical Propagation delay time is 1nS

- Fan-out is typically about 25. Low Impedance emitter-follower outputs

5.4: ECL Advantages
- The transistors never saturate and so switching speed is very high., which makes ECL a little faster than advanced Schottky TTL

- An ECL logic block usually produces an output and its complement. This eliminates the need for inverters.

- The total current flow in an ECL circuit remains relatively constant regardless of its logic state.
  - Steady current requirement ensures no noise spikes during transitions. Output signals very clean

5.4: ECL Disadvantages
- Low noise margins, approx 250mV. Difficult to use in noisy environments such as automobile, RF, etc.

- High power dissipation due to constant current flows. 
  \[ P_D = 25 \text{mW/gate} \]. Higher than 74 TTL series.

- Negative power supply need. Makes circuit very expensive if interfaced to non-ECL components such as TTL, CMOS
5.5 Integrated Injection Logic (I\textsuperscript{2}L)

- A digital circuit composed of bipolar transistors. It has relatively fast switching speeds and utilizes little power.
- Similar speed to TTL but less power.

Q1 (PNP) is always on. The current passing into base of Q2 depends on the resistor value, $R_{ext}$.

The input connection is either high-impedance floating (Logic 1) or is connected to 0V as a current sink (Logic 0).

When input is open (Hi-Z), current I flows into base of Q2, switching Q2 ON and pulling the output to ground, $Out = 0$. If the input is shorted to 0V (logic0), then I is shunted away from Q2’s base, switching Q2 off to give a high impedance o/p(logic1).

- Circuit is IIL inverter.
When both inputs are 0, P will be Hi-Z turning Q3 ON, F = 0
When either input is 1, P will be pulled to 0. Q3 will be off and F will be Hi-Z (1).

<table>
<thead>
<tr>
<th>A</th>
<th>Q1</th>
<th>B</th>
<th>Q2</th>
<th>P</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>OFF</td>
<td>0</td>
<td>OFF</td>
<td>Hi-Z</td>
<td>0V</td>
</tr>
<tr>
<td>0</td>
<td>OFF</td>
<td>1</td>
<td>ON</td>
<td>0V</td>
<td>Hi-Z</td>
</tr>
<tr>
<td>1</td>
<td>ON</td>
<td>0</td>
<td>OFF</td>
<td>0V</td>
<td>Hi-Z</td>
</tr>
<tr>
<td>1</td>
<td>ON</td>
<td>1</td>
<td>ON</td>
<td>0V</td>
<td>Hi-Z</td>
</tr>
</tbody>
</table>

F = A + B
Remove Q3 to make an NOR operation

Properties of IIL:
- No internal resistors needed: Larger integration possible
  - 10 times the component density than TTL
- Speed & Power can be tailored for application
  - Low power application: Large $R_{ext} \Rightarrow t_p \approx 100\text{ns}, P_D \approx 5\text{nW}$
  - High Speed application: Small $R_{ext} \Rightarrow t_p \approx 5\text{ns}, P_D \approx 5\text{mW}$
- Can be used in wired-AND data bussing
5.6 MOS Technology

MOSFET : Metal Oxide Semiconductor Field Effect Transistor

- When $V_{GS} < V_{TH}$ (ie $V_{GS}=0$), Reverse biased p-n junction between S and D. No electron flow between source and drain. MOSFET is OFF.
- When $V_{GS} > V_{TH}$, Electrons are attracted to gate creating n-type conductive channel is formed under oxide. MOSFET is ON.
- PMOS is opposite. Requires negative $V_{GS}$ voltage to draw holes to gate.
5.6.1 NMOS Logic

- Use only N-Channel MOSFETs
  - When $V_{GS} = V_{DD}$, $R_{on} = 1K\Omega$
  - When $V_{GS} = 0$, $R_{off} = 10^{10}\Omega$

NMOS NAND Gate

$\begin{array}{|c|c|c|}
\hline
V_{in} & MOSFET & V_{out} \\
\hline
0V & R_{off} = 10^{10}\Omega & V_{DD} \\
V_{DD} & R_{on} = 10^{3}\Omega & \sim0V \\
\hline
\end{array}$

$\begin{array}{|c|c|c|}
\hline
A & B & F \\
\hline
0V & 0V & V_{DD} \\
0V & V_{DD} & V_{DD} \\
V_{DD} & 0V & V_{DD} \\
V_{DD} & V_{DD} & 0V \\
\hline
\end{array}$
NMOS NOR Gate

NMOS Properties
- Speed: ~ 50ns
- Power: ~ 0.1mW/gate
- Noise Margin ≈ 1.5V when $V_{DD} = 5V$
- Fan Out > 50

NMOS Advantages:
- Simple Fabrication Process
  - Only Single Gate is Needed
- High Density:
  - Only loading “resistor” needed

NMOS Disadvantages:
- Static Charge Build-Up
  - Need circuitry to protect against.
- Slow 0→1 Change
- High Power Consumption
  - When output is low, Current flows across NMOS gate => Power consumed when idle.
5.7 CMOS Logic

- Utilises both NMOS and PMOS gates together
  - Complementary and Symmetrical Design

![CMOS Logic Diagram]

<table>
<thead>
<tr>
<th>$V_{IN}$</th>
<th>$Q1$</th>
<th>$Q2$</th>
<th>$V_{OUT}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0V</td>
<td>ON($10^3\Omega$)</td>
<td>OFF($10^{10}\Omega$)</td>
<td>$V_{DD}$</td>
</tr>
<tr>
<td>$V_{DD}$</td>
<td>OFF($10^{10}\Omega$)</td>
<td>ON($10^3\Omega$)</td>
<td>0V</td>
</tr>
</tbody>
</table>

$\therefore V_{OUT} = \overline{V_{IN}}$
5.7.2 CMOS NOR Gate

When $A=0V$ and $B=0V$
$\Rightarrow$ P0 and P1 are ON. N0 and N1 are OFF.
- $F$ is pulled high to $V_{DD}$

When either $A$ or $B$ is $V_{DD}$
$\Rightarrow$ Either N0 or N1 will be ON
- $F$ is pulled low to GND

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>0V</td>
<td>0V</td>
<td>$V_{DD}$</td>
</tr>
<tr>
<td>0V</td>
<td>$V_{DD}$</td>
<td>0V</td>
</tr>
<tr>
<td>$V_{DD}$</td>
<td>0V</td>
<td>0V</td>
</tr>
<tr>
<td>$V_{DD}$</td>
<td>$V_{DD}$</td>
<td>0V</td>
</tr>
</tbody>
</table>

$F = A + B$
5.7.3 CMOS NAND Gate

- N0 and N1 must be ON to connect F to GND.
  ⇒ A and B must be \( V_{DD} \)
  - F is pulled to GND

When either A or B is 0V
  ⇒ Either P0 or P1 is ON and either N0 or N1 blocks path to GND
  - F is pulled to \( V_{DD} \)

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>P0</th>
<th>P1</th>
<th>N0</th>
<th>N1</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>0V</td>
<td>0V</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>( V_{DD} )</td>
</tr>
<tr>
<td>0V</td>
<td>( V_{DD} )</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>( V_{DD} )</td>
</tr>
<tr>
<td>( V_{DD} )</td>
<td>0V</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
<td>( V_{DD} )</td>
</tr>
<tr>
<td>( V_{DD} )</td>
<td>( V_{DD} )</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>0V</td>
</tr>
</tbody>
</table>

\[
F = \overline{AB}
\]
\[ Y = \overline{A B} + C \]
CMOS Properties

Loading Resistor not needed

Noise Margin: \( V_{IL}(\text{max}) = 30\% \text{ of } V_{DD} \)
\( V_{IH}(\text{min}) = 70\% \text{ of } V_{DD} \)

\( V_{OH}(\text{min}) = V_{DD} - 0.05V, V_{OL}(\text{max}) = 0.05V \)

Noise Margin = 30\% of \( V_{DD} \)

Speed:
Limited by circuit capacitance
Initially not as fast as TTL since input capacitance is higher but can be minimised.

Fan-out: MOSFET is voltage controlled device unlike BJT. Each transistor draws vary little current allowing large Fan-out. However each additional gate input causes an increase output capacitance and the delay of the circuit.

CMOS Power
Always one transistor ‘blocking’ path to ground

Ideal CMOS would only dissipate when switching from high to low or high to low.

Dynamic power consumption caused by changes in circuit capacitances. Gate, Source, Drain and Wire capacitances must be charged and discharged during switching.

Real CMOS also dissipates small amounts of power when idle…

Static Power due to leakage
Gate->source leakage
Source->Drain leakage
Reverse Bias leakage
At smaller technologies (<130nm) the leakage is higher as insulation Oxide is thinner...

Power Consumption Ratios for Altera FPGA

At 130nm: Dynamic=81%, Static=7%
At 90nm: Dynamic=66%, Static=28%

**Short-Circuit Power**: When switching logic level the input is floating, both transistors are on for a small period of time creating Path to ground. Must account for floating inputs to prevent short circuit.

**Comparison of logic families:**

<table>
<thead>
<tr>
<th>Family</th>
<th>Basic gate</th>
<th>Fan-out (gate)</th>
<th>Pd (mW/gate)</th>
<th>Noise immunity</th>
<th>Prop. delay (ns/gate)</th>
<th>Clock (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TTL</td>
<td>NAND</td>
<td>10</td>
<td>10</td>
<td>VG</td>
<td>10</td>
<td>35</td>
</tr>
<tr>
<td>TTL-H</td>
<td>NAND</td>
<td>10</td>
<td>22</td>
<td>VG</td>
<td>6</td>
<td>50</td>
</tr>
<tr>
<td>TTL-L</td>
<td>NAND</td>
<td>20</td>
<td>1</td>
<td>VG</td>
<td>33</td>
<td>3</td>
</tr>
<tr>
<td>TTL-LS</td>
<td>NAND</td>
<td>20</td>
<td>2</td>
<td>VG</td>
<td>9.5</td>
<td>45</td>
</tr>
<tr>
<td>TTL-S</td>
<td>NAND</td>
<td>10</td>
<td>19</td>
<td>VG</td>
<td>3</td>
<td>125</td>
</tr>
<tr>
<td>TTL-AS</td>
<td>NAND</td>
<td>40</td>
<td>10</td>
<td>VG</td>
<td>1.5</td>
<td>175</td>
</tr>
<tr>
<td>TTL-ALS</td>
<td>NAND</td>
<td>20</td>
<td>1</td>
<td>VG</td>
<td>4</td>
<td>50</td>
</tr>
<tr>
<td>ECL 10K</td>
<td>OR-NOR</td>
<td>25</td>
<td>40-55</td>
<td>P</td>
<td>2</td>
<td>&gt;60</td>
</tr>
<tr>
<td>ECL 100K</td>
<td>OR-NOR</td>
<td>??</td>
<td>40-55</td>
<td>P</td>
<td>0.75</td>
<td>600</td>
</tr>
<tr>
<td>MOS</td>
<td>NAND</td>
<td>20</td>
<td>0.2-10</td>
<td>G</td>
<td>300</td>
<td>2</td>
</tr>
<tr>
<td>74C</td>
<td>NOR/NAND</td>
<td>50</td>
<td>0.01/1</td>
<td>VG</td>
<td>70</td>
<td>10</td>
</tr>
<tr>
<td>74HC</td>
<td>NOR/NAND</td>
<td>20</td>
<td>0.0025/0.6</td>
<td>VG</td>
<td>18</td>
<td>60</td>
</tr>
<tr>
<td>74HCT</td>
<td>NOR/NAND</td>
<td>20</td>
<td>0.0025/0.6</td>
<td>VG</td>
<td>18</td>
<td>60</td>
</tr>
<tr>
<td>74AC</td>
<td>NOR/NAND</td>
<td>50</td>
<td>0.005/0.75</td>
<td>VG</td>
<td>5.25</td>
<td>100</td>
</tr>
<tr>
<td>74ACT</td>
<td>NOR/NAND</td>
<td>50</td>
<td>0.005/0.75</td>
<td>VG</td>
<td>4.75</td>
<td>100</td>
</tr>
</tbody>
</table>

- Figures of merit can be calculated as product of propagation delay and power dissipation Pd
- For CMOS, Pd is static/dynamic(1MHz) and figure of merit is calculated for each. TotalPd=staticPd + DynamicPd
- VG=VeryGood G=Good P=Poor
5.7 CMOS/TTL Interfacing: TTL driving CMOS

When interfacing different types of IC’s, we must check that the driving device can meet the current and voltage requirements of the load device. Examination of Table 1 indicates that the input current values for CMOS are extremely low compared with the output current capabilities of any TTL series. Thus, TTL has no problem meeting the CMOS input current requirements.

There is a problem, however, when we compare the TTL output voltages with the CMOS input voltage requirements. Table 2 shows that $V_{OH}$ (Min) of every TTL series is too low when compared with the $V_{IH}$ (Min) requirement of the 4000B, 74HC, and the 74AC series. For these situations, something must be done to raise the TTL output voltage to an acceptable level for CMOS.

Table 1

<table>
<thead>
<tr>
<th>Parameter</th>
<th>4000B</th>
<th>74HC/HCT</th>
<th>74AC/ACT</th>
<th>74AHC/AHCT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{IH}$ (max)</td>
<td>$1 \mu A$</td>
<td>$1 \mu A$</td>
<td>$1 \mu A$</td>
<td>$1 \mu A$</td>
</tr>
<tr>
<td>$I_{IL}$ (max)</td>
<td>$1 \mu A$</td>
<td>$1 \mu A$</td>
<td>$1 \mu A$</td>
<td>$1 \mu A$</td>
</tr>
<tr>
<td>$I_{OH}$ (max)</td>
<td>0.4mA</td>
<td>4mA</td>
<td>24mA</td>
<td>8mA</td>
</tr>
<tr>
<td>$I_{OL}$ (max)</td>
<td>0.4mA</td>
<td>4mA</td>
<td>24mA</td>
<td>8mA</td>
</tr>
</tbody>
</table>

Table 2

<table>
<thead>
<tr>
<th>Parameter</th>
<th>4000B</th>
<th>74HC</th>
<th>74HCT</th>
<th>74AC</th>
<th>74ACT</th>
<th>74AHC</th>
<th>74AHCT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$ (min)</td>
<td>3.5</td>
<td>3.5</td>
<td>2.0</td>
<td>3.5</td>
<td>2.0</td>
<td>3.85</td>
<td>2.0</td>
</tr>
<tr>
<td>$V_{IL}$ (max)</td>
<td>1.5</td>
<td>1.0</td>
<td>0.8</td>
<td>1.5</td>
<td>0.8</td>
<td>1.65</td>
<td>0.8</td>
</tr>
<tr>
<td>$V_{OH}$ (min)</td>
<td>4.95</td>
<td>4.9</td>
<td>4.9</td>
<td>4.9</td>
<td>4.9</td>
<td>4.4</td>
<td>3.15</td>
</tr>
<tr>
<td>$V_{OL}$ (max)</td>
<td>0.05</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td>0.44</td>
<td>0.1</td>
</tr>
<tr>
<td>$V_{NH}$</td>
<td>1.45</td>
<td>1.4</td>
<td>2.9</td>
<td>1.4</td>
<td>2.9</td>
<td>0.55</td>
<td>1.15</td>
</tr>
<tr>
<td>$V_{NL}$</td>
<td>1.45</td>
<td>0.9</td>
<td>0.7</td>
<td>1.4</td>
<td>0.7</td>
<td>1.21</td>
<td>0.7</td>
</tr>
</tbody>
</table>
The most common solution to this interface problem is shown in figure 1, where the TTL output is connected to +5V with a pull-up resistor. The presence of the pull-up resistor causes the TTL output to rise to approximately 5V in the High state, thereby providing an adequate CMOS input voltage level. This pull-up resistor is not required if the CMOS device is a 74HCT or a 74ACT because these series are designed to accept TTL outputs directly, as Table 2 shows.

**Figure 1 – External pull-up resistor is used when TTL drives CMOS**

![Pull-up Resistor Diagram](image)

**CMOS Driving TTL in the HIGH State**

Table 2 shows that CMOS outputs can easily supply enough voltage ($V_{OH}$) to satisfy the TTL input requirement in the HIGH state ($V_{IH}$). Table 1 shows that CMOS outputs can supply more than enough current ($I_{OH}$) to meet the TTL input current requirements ($I_{IH}$). Thus, no special consideration is needed for the HIGH state.

**CMOS Driving TTL in the LOW State**

Table 1 shows that TTL inputs have a relatively high input current in the LOW state, ranging from 100µA to 2 mA. The 74HC and 74HCT series can sink up to 4 mA, and would have no trouble driving a single TTL load of any series. The 4000B series, however, is much more limited. Its low $I_{OL}$ capability is not sufficient to drive even one input of the 74 or 74AS series. The 74AHC series has output drive comparable to that of the 74LS series.